CLAIMS

What is claimed is:

1. A latch based random access memory comprising:

an input data register;

an input data buffer coupled to the input data register;

a latch array coupled to the input data buffer; and

a latch array bypass multiplexer for selecting one of the input data buffer and the latch array to generate a first data output of the latch based random access memory from the input data buffer during logic scan testing and a second data output of the latch based random access memory from the latch array during memory scan testing in response to a memory scan mode signal.

2. The latch based random access memory of Claim 1 further comprising:

a read address register; and

a read address multiplexer coupled to the read address register for selecting one of a logic scan address and a memory scan address in response to the memory scan mode signal.

3. The latch based random access memory of Claim 2 further comprising:

a write enable register; and

a clock signal multiplexer coupled to the read address register and the write enable register for selecting one of a scan test clock signal and an application specific clock signal in response to a scan mode signal.

4. The latch based random access memory of Claim 3 further comprising bypass logic for controlling the latch array bypass multiplexer in response to the memory scan mode signal and the scan mode signal.

5. The latch based random access memory of Claim 3 further comprising a lockup latch coupled to the read address register for providing a minimum hold time for the write enable register during scan testing of the latch based random access memory.

6. The latch based random access memory of Claim 2 further comprising a lockup latch coupled to the input data register for providing a minimum hold time during scan testing of the latch based random access memory.

7. A method of scan testing a latch based random access memory in an integrated circuit die comprising steps of:

(a) modifying a latch based memory to include a latch array bypass multiplexer for selecting one of an input data buffer of the latch based random access memory

and a latch array of the latch based random access memory for generating a first data output of the latch based random access memory from the input data buffer during logic scan testing and a second data output of the latch based random access memory from the latch array during memory scan testing in response to a memory scan mode signal;

(b) asserting the memory scan mode signal during a memory scan test; and

(c) removing the memory scan mode signal during a logic scan test.

8. The method of Claim 7 further comprising a step of selecting one of a logic scan address and a memory scan address for coupling to a read address register of the latch based random access memory in response to the memory scan mode signal.

9. The method of Claim 8 further comprising a step of selecting one of a scan test clock signal and an application-specific clock signal for coupling to the read address register and a write address register of the latch based random access memory in response to a scan mode signal.

10. The method of Claim 9 further comprising a step of controlling the latch array bypass multiplexer in response to the scan mode signal.

11. The method of Claim 7 further comprising a step of providing a minimum hold time during scan testing of the latch based random access memory.

12. The method of Claim 7 wherein step (b) further comprises bypassing logic chains surrounding the latch based random access memory during a memory scan test.

13. The method of Claim 7 wherein step (c) further comprises bypassing the latch array during a logic scan test.